IN THE CLAIMS

Claims 1-33 (cancelled).

34. (currently amended) An intermediary of a semiconductor device comprising:

a semiconductor substrate formed with a first recessed region having a lower surface depressed with respect to a major surface of the semiconductor substrate;

a pillar region comprised of a plurality of pillars comprising a dielectric material formed in the first recessed region and extending from the lower surface of the first recessed surface, wherein a plurality of voids is within the pillar region; and

a plurality of polysilicon cap layers having a lower surface formed adjoining ~~upper surfaces of the pillar region~~ and overlying each of the plurality of pillars, wherein the lower surface of the plurality of polysilicon cap layers is aligned with a top surface of each of the plurality of voids, and wherein sidewall surfaces of the plurality of pillars are devoid of the polysilicon cap layers, and wherein the pillar region and the plurality of polysilicon cap layers are configured to form an isolation region having reduced substrate capacitance.

35. (currently amended) The intermediary of claim 34, wherein each of the plurality of polysilicon cap layers has a thickness of about 4,500 angstroms.

36. (previously presented) The intermediary of claim 34, wherein the upper surfaces of the pillar region are

recessed below the major surface of the semiconductor substrate.

37. (previously presented) The intermediary of claim 36, wherein the upper surfaces are recessed a distance of about 0.5 microns.

38. (previously presented) The intermediary of claim 34, wherein the pillar region comprises deposited silicon dioxide.

39. (previously presented) The intermediary of claim 34, wherein the pillar region comprises a matrix of a plurality of pillars.

40. (currently amended) The intermediary of claim 39, wherein at least a portion of the matrix of a plurality of pillars includes pillars having a generally rectangular shape.

41. Cancelled.

42. (previously presented) The intermediary of claim 34, wherein the pillar region extends a distance of about 4.5 micrometers from the lower surface of the first recessed region and has a dielectric constant of about 3.5.